Notice of Allowability	Application No.	Applicant(s)	
	09/904,432	RAGHAVAN, SREEN	
	Examiner	Art Unit	
	Lawrence B. Williams	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed 21 February 2007*.

2. ☒ The allowed claim(s) is/are *1-11, 13-17, 21-30, 32-33, 35, 38, 40-43, 46-50, renumbered as 1-11, 12-16, 17-26, 27-28, 29, 30, 31-34, 35-39, respectively*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Gary Edwards on 21 June 2007.

The application has been amended as follows:

1.) Cancel claim 44.

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance: The instant application discloses a method for communicating and a serializer/deserializer communications system. A search of prior art records has failed to teach or suggest alone or in combination:

" a serializer/deserializer communications system, comprising: a transmitter, the transmitter coupled to receive N parallel bits of data and transmit the N parallel bits of data into K frequency separated channels on a single conducting differential transmission medium, where N and K are integers each greater than one, the N parallel bits being transmitted into the K frequency separated channels of the serializer/deserializer system synchronously; and a receiver coupled to receive a sum signal that includes signals from each of the K frequency separated channels from the single conducting differential transmission medium and recover the N parallel bits of data, wherein the receiver includes K demodulators, each of the K demodulators receiving signals on one of the K frequency separated channels, at least one of the K demodulators including an analog down converter that down converts the signal corresponding to that channel associated with the at least one of the demodulators to a base-band signal in a single step; an analog-to-digital converter coupled to receive the base-band signal from the analog down converter and generate a digitized base-band signal; an equalizer circuit coupled to receive the digitized base-band signal and create an equalized symbol; and a decoder that synchronously retrieves the equalized symbol and retrieves bits associated with the at least one of the K demodulators" as disclosed in claim 1.

" a method of communicating between components over a conducting differential transmission medium, comprising: synchronously serializing N bits into K subsets of bits;

encoding each of the K subsets of bits to form encoded subsets of bits; mapping each of the K encoded subsets of bits onto a symbol set to generate K symbols representing each of the K subsets of bits; converting each of the K symbols to K analog signals; up-converting each of the K analog signals in a single analog up-conversion step to form K up-converted signals corresponding with a set of K carrier frequencies; summing the K up-converted signals representing each of the K subsets of bits to generate a transmit sum signal; and coupling the transmit sum signal to the single conducting differential transmission medium; receiving a receive sum signal from the single conducting differential transmission medium, the receive sum signal being the transmit sum signal after transmission through the single conducting differential transmission medium; down-converting the received sum signal in a single analog down-conversion step for each of the K carrier frequencies into a set of K signals at a base band frequency; digitizing each of the set of K signals to form K digitized signals; equalizing each of the K digitized signals to receive K equalized symbols; and decoding each of the K synchronously equalized symbols to reconstruct the K subsets of bits; and parsing K subsets of bits into N deserialized bits" as disclosed in claim 27.

"a transceiver chip for a serializer/deserializer system, comprising: a transmitter portion, the transmitter portion coupled to receive N parallel bits of data and transmit the N parallel bits of data into a first set of K frequency separated channels on a first single conducting differential transmission medium, the N parallel bits being transmitted into the K frequency separated channels of the serializer/deserializer system synchronously where N and K are integers each greater than one; and a receiver portion coupled to receive data from a second set of K frequency separated channels from a second single conducting differential transmission medium and

recover a second N parallel bits of data, wherein the receiver portion includes K demodulators, each of the K demodulators coupled to receive a signal from the second single conducting differential transmission medium, the signal being a transmit sum signal transmitted through the second single conducting differential transmission medium, and retrieving one of the K subsets of data bits and a bit parsing circuit that receives each of the K subsets of data bits from the K demodulators and reconstructs the N data bits transmitted by the transmitter, and wherein at least one of the K demodulators comprises an analog down-conversion circuit that receives the signal from the second single conducting differential transmission medium and generates a symbol by converting the signal at the carrier frequency appropriate for the one of the K demodulators, an analog to digital converter coupled to digitize the symbol from the analog down conversion circuit, an equalizer circuit coupled to receive the digitized symbol from the analog to digital converter and create an equalized symbol; and a decoder which receives the equalized symbol and synchronously retrieves the one of the K subsets of bits associated with the at least one of the K demodulators" as disclosed in claim 46.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ghayour Mohammad can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw

June 21, 2007

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER